

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N3819

N-channel J-FET

FEATURES

- Low cost
- Specified at 100 MHz
- Automatic insertion package.

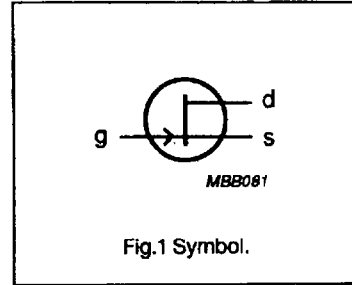
DESCRIPTION

N-channel junction field-effect transistor in a plastic TO-92 envelope. It is intended for use in general purpose amplifiers and for analog switching.

PINNING - TO-92

PIN	DESCRIPTION
1	drain
2	gate
3	source

PIN CONFIGURATION



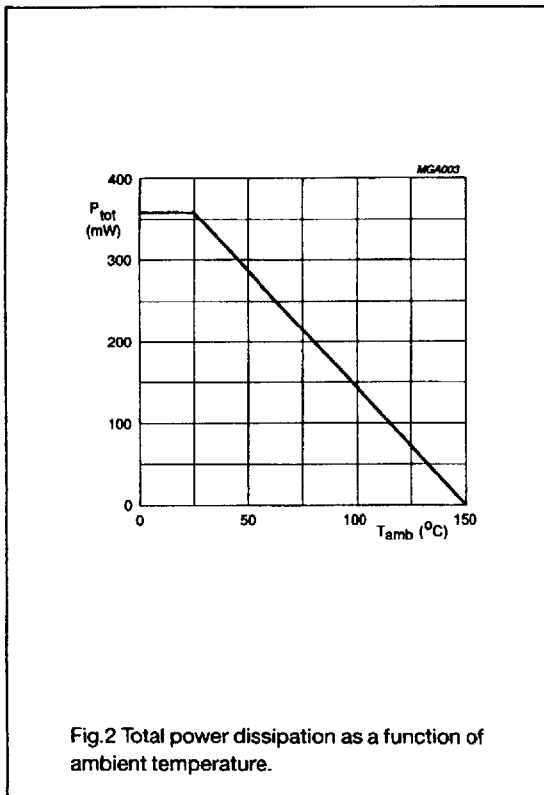
N-channel J-FET**2N3819****LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage	open drain $I_D = 0$	-	25	V
V_{DGO}	drain-gate voltage	open source $I_S = 0$	-	25	V
I_G	gate current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^\circ\text{C}$	-	360	mW
T_{stg}	storage temperature range		-65	150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient	347	K/W



N-channel J-FET**2N3819****CHARACTERISTICS** $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{(BR)GS}$	gate-source breakdown voltage	$V_{DS} = 0$ $-I_G = 1\text{ }\mu\text{A}$	25	-	V
$-I_{GSS}$	gate-source leakage current	$-V_{GS} = 15\text{ V}$ $V_{DS} = 0$	-	2	nA
		$-V_{GS} = 15\text{ V}$ $V_{DS} = 0$ $T_{amb} = 100\text{ }^{\circ}\text{C}$	-	2	μA
I_{DSS}	drain-source current	$V_{GS} = 0$ $V_{DS} = 15\text{ V}$	2	20	mA
$-V_{GS}$	gate-source voltage	$I_D = 200\text{ }\mu\text{A}$ $V_{DS} = 15\text{ V}$	0.5	7.5	V
$-V_{(P)GS}$	gate-source cut-off voltage	$I_D = 2\text{ nA}$ $V_{DS} = 15\text{ V}$	-	8	V
$ y_{fs} $	transfer admittance	$V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ kHz}$	2	6.5	mS
$ y_{fs} $	transfer admittance	$V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 100\text{ MHz}$	1.6	-	mS
$ y_{os} $	output admittance	$V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ kHz}$	-	50	μS
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	-	8	pF
C_{rss}	feedback capacitance	$V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	-	4	pF

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PACKAGE OUTLINE

