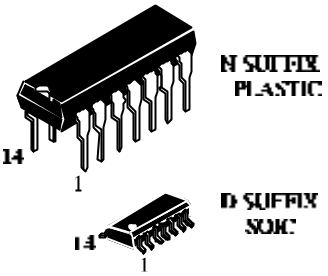
8-Bit Serial-Input/Parallel-Output Shift Register

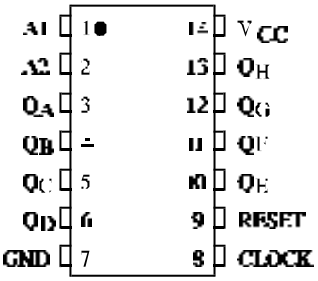
This 8-bit shift register features gated serial inputs and an asynchronous reset. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip flop to the low level at the next clock pulse. A high level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered clocking occurs or the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

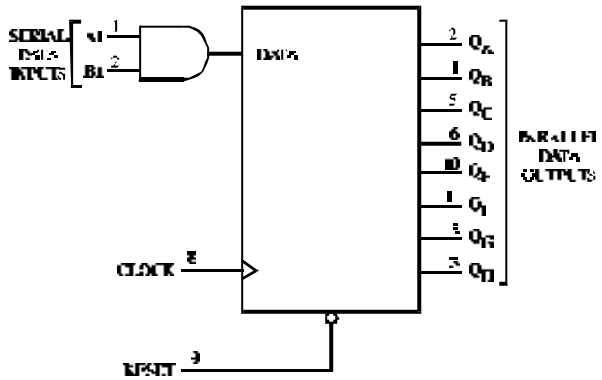


ORDERING INFORMATION
SL74LS164N Plastic
SL74LS164D SOIC
T_A =0° to 70°C
for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

FUNCTION TABLE

Inputs			Outputs
Reset	Clock	A1 A2	Q_A Q_B ... Q_H
L	X	X X	L L ... L
H	↓	X X	no change
H	↑	H D	D Q_{An} ... Q_{Gn}
H	↑	D H	D Q_{An} ... Q_{Gn}
H	↑	L L	L Q_{An} ... Q_{Gn}

D = data input
X = don' t care
Q_{An} - Q_{Gn} = data shifted from the previous stage on a rising edge at the clock input.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	7.0	V
V_{OUT}	Output Voltage	5.5	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	High Level Input Voltage	2.0		V
V_{IL}	Low Level Input Voltage		0.8	V
I_{OH}	High Level Output Current		-0.4	mA
I_{OL}	Low Level Output Current		8.0	mA
T_A	Ambient Temperature Range	0	+70	°C
f_{clock}	Clock Frequency	0	25	MHz
t_{su}	Setup Time, A1 or A2 to Clock	15		ns
t_h	Hold Time, Clock to A1 or A2	5		ns
t_w	Pulse Width, Clock	20		ns
t_w	Pulse Width, Reset	20		ns
t_{rec}	Recovery Time	5		ns

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = min, I_{IN} = -18 mA		-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = min, I_{OH} = -0.4 mA	2.7		V
V_{OL}	Low Level Output Voltage	V_{CC} = min, I_{OL} = 4 mA		0.4	V
		V_{CC} = min, I_{OL} = 8 mA		0.5	
I_{IH}	High Level Input Current	V_{CC} = max, V_{IN} = 2.7 V		20	mA
		V_{CC} = max, V_{IN} = 7.0 V		0.1	mA
I_{IL}	Low Level Input Current	V_{CC} = max, V_{IN} = 0.4 V		-0.4	mA
I_O	Output Short Circuit Current	V_{CC} = max, V_O = 0 V (Noote 1)	-20	-100	mA
I_{CC}	Supply Current	V_{CC} = max (Note 2)		27	mA

Note 1: Not more than one output should be shorted at a time, and duration should not exceed one second.

Note 2: I_{CC} is measured with outputs open, serial inputs grouned, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied.

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2 kΩ, t_r =15 ns, t_f = 6.0 ns)

Symbol	Parameter	Min	Max	Unit
t_{PLH}	Propagation Delay Time, Clock to Q		27	ns
t_{PHL}	Propagation Delay Time, Clock to Q		32	ns
t_{PHL}	Propagation Delay Time, Reset to Q		36	ns
t_{su}	Setup Time, A1 or A2 to Clock	15		ns
t_h	Hold Time, Clock to A1 or A2	5		ns
t_w	Pulse Width, Clock	20		ns
t_w	Pulse Width, Reset	20		ns

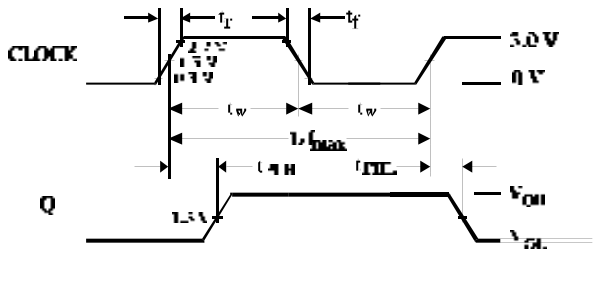


Figure 1. Switching Waveforms

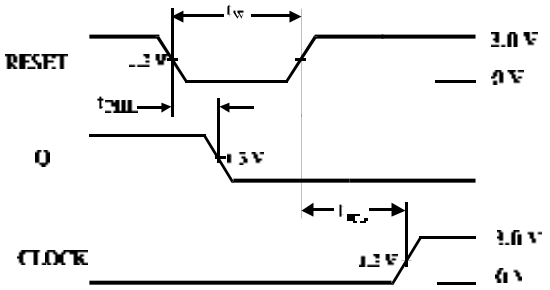


Figure 2. Switching Waveforms

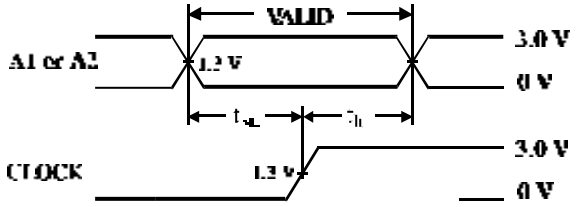
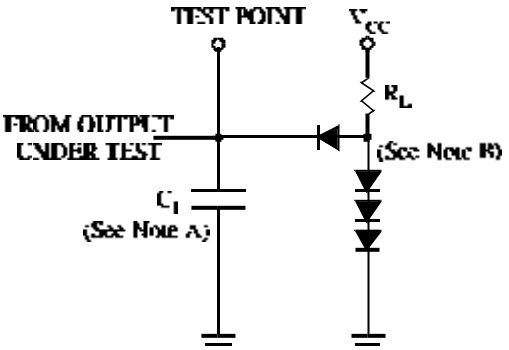


Figure 3. Switching Waveform



NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 4. Test Circuit

TIMING DIAGRAM