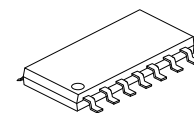


**CD4011B****CMOS IC****QUAD 2-INPUT NAND
BUFFERED B SERIES GATE**■ **DESCRIPTION**

The **UTC CD4011B** contains four independent 2-input NAND gates which perform the function $Y = \overline{A \bullet B}$ in positive logic.

■ **FEATURES**

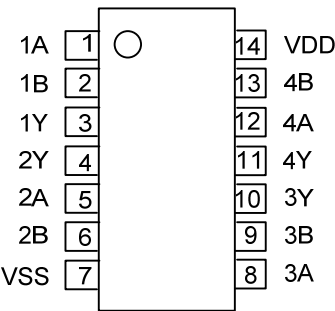
- * 5V-10V-15V Parametric Ratings
- * Quad 2-Input NAND Gate
- * Symmetrical Output Characteristics
- * Maximum Input Current of 1uA at 15V Over Full Package Temperature Range
- * Low Power TTL:
Fan Out of 2 Driving 74L or 1 Driving 74LS Compatibility

**SOP-14**■ **ORDERING INFORMATION**

Ordering Number		Package	Packing
Lead Free	Halogen Free		
CD4011BL-S14-R	CD4011BG-S14-R	SOP-14	Tape Reel

CD4011BL-S14-R (1) Packing Type (2) Package Type (3) Lead Plating	(1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free, L: Lead Free
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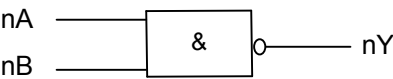
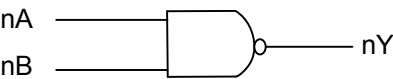
PIN CONFIGURATION



FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
H	L	H
L	H	H
L	L	H

LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING(unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VDD	-0.5 ~ 18	V
Input Voltage	V(nA,nB)	-0.5 ~ VDD +0.5	V
Output Voltage	V(nY)	-0.5 ~ VDD +0.5	V
Storage Temperature	T _{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VDD	3 ~ 15	V
Operating Temperature	T _{OP}	-55 ~ 125	°C

■ ELECTRICAL CHARACTERISTICS(T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V _{IH}	VDD= 5V, VO=0.5V	3.5	3		V
		VDD= 10V, VO=1.0V	7.0	6		
		VDD= 15V, VO=1.5V	11.0	9		
Low-Level Input Voltage	V _{IL}	VDD= 5V, VO=4.5V		2	1.5	V
		VDD= 10V, VO=9.0V		4	3.0	
		VDD= 15V, VO=13.5V		6	4.0	
High-Level Output Voltage	V _{OH}	VDD= 5V, I _O < 1μA	4.95	5		V
		VDD= 10V, I _O < 1μA	9.95	10		
		VDD= 15V, I _O < 1μA	14.95	15		
Low-Level Output Voltage	V _{OL}	VDD= 5V, I _O < 1μA		0	0.05	V
		VDD= 10V, I _O < 1μA		0	0.05	
		VDD= 15V, I _O < 1μA		0	0.05	
High-Level Output Current (NOTE)	I _{OH}	VDD= 5V, VO=4.6V	-0.51	-0.88		mA
		VDD= 10V, VO=9.5V	-1.3	-2.25		
		VDD= 15V, VO=13.5V	-3.4	-8.8		
Low-Level Output Current (NOTE)	I _{OL}	VDD= 5V, VO=0.4V	0.51	0.88		mA
		VDD= 10V, VO=0.5V	1.3	2.25		
		VDD= 15V, VO=1.5V	3.4	8.8		
Input Leakage Current	I _{I(LEAK)}	VDD= 15V, V _{IN} = VDD or GND			0.1	μA
Quiescent Supply Current	I _Q	VDD= 5V, V _{IN} = VDD or VSS, I _{OUT} = 0		0.004	0.25	μA
		VDD= 10V, V _{IN} = VDD or VSS, I _{OUT} = 0		0.005	0.5	
		VDD= 15V, V _{IN} = VDD or VSS, I _{OUT} = 0		0.006	1.0	

Note: I_{OL} and I_{OH} are tested one output at a time

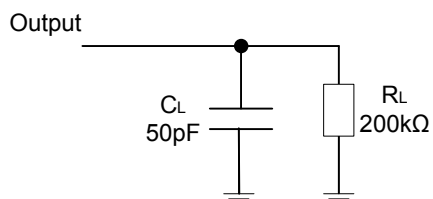
■ SWITCHING CHARACTERISTICS($T_A=25^\circ\text{C}$, Input: $t_R=t_F=20\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	VDD=5V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		85	250	ns
		VDD=10V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	100	
		VDD=15V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		30	70	
	t_{PHL}	VDD=5V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		120	250	
		VDD=10V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	
		VDD=15V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		35	70	
Transition Time	t_{TLH}	VDD=5V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		90	200	ns
	t_{THL}	VDD=10V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	
		VDD=15V, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	80	

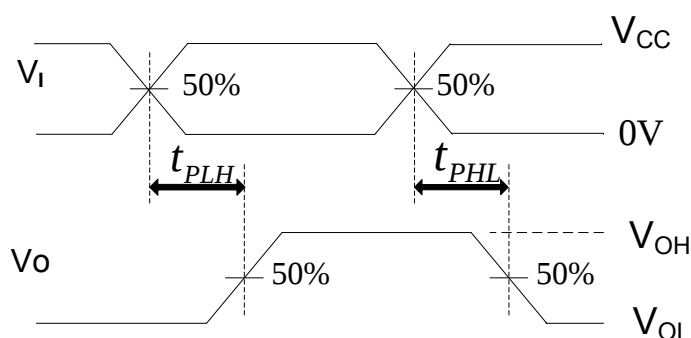
■ OPERATING CHARACTERISTICS($T_a=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{in}	Any Input		5	7.5	pF
Power Dissipation Capacitance	C_{pd}	Any Gate		14		

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



Propagation Delay Times

Note: C_L includes probe and jig capacitance.

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